Selected instructions from the MIPS instruction sec. Excerpted from <https://en.wikipedia.org/wiki/MIPS_architecture>

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| --- | --- | --- | --- | --- | --- | --- |
| **Instruction name** | **Mnemonic** | **Format** | **Encoding** | | | |
| Load Byte | LB | I | 3210 | rs | rt | offset |
| Load Word | LW | I | 3510 | rs | rt | offset |
| Load Byte Unsigned | LBU | I | 3610 | rs | rt | offset |
| Store Byte | SB | I | 4010 | rs | rt | offset |
| Store Word | SW | I | 4310 | rs | rt | offset |

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| **Instruction name** | **Mnemonic** | **Format** | **Encoding** | | | | | |
| Add | ADD | R | 010 | rs | rt | rd | 010 | 3210 |
| Add Unsigned | ADDU | R | 010 | rs | rt | rd | 010 | 3310 |
| Subtract | SUB | R | 010 | rs | rt | rd | 010 | 3410 |
| Subtract Unsigned | SUBU | R | 010 | rs | rt | rd | 010 | 3510 |
| And | AND | R | 010 | rs | rt | rd | 010 | 3610 |
| Or | OR | R | 010 | rs | rt | rd | 010 | 3710 |
| Exclusive Or | XOR | R | 010 | rs | rt | rd | 010 | 3810 |
| Nor | NOR | R | 010 | rs | rt | rd | 010 | 3910 |
| Set on Less Than | SLT | R | 010 | rs | rt | rd | 010 | 4210 |
| Set on Less Than Unsigned | SLTU | R | 010 | rs | rt | rd | 010 | 4310 |
| Add Immediate | ADDI | I | 810 | rs | rt | immediate | | |
| Add Immediate Unsigned | ADDIU | I | 910 | rs | rt | immediate | | |
| Set on Less Than Immediate | SLTI | I | 1010 | rs | rt | immediate | | |
| Set on Less Than Immediate Unsigned | SLTIU | I | 1110 | rs | rt | immediate | | |
| And Immediate | ANDI | I | 1210 | rs | rt | immediate | | |
| Or Immediate | ORI | I | 1310 | rs | rt | immediate | | |
| Exclusive Or Immediate | XORI | I | 1410 | rs | rt | immediate | | |
| Load Upper Immediate | LUI | I | 1510 | 010 | rt | immediate | | |

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| **Instruction name** | **Mnemonic** | **Format** | **Encoding** | | | | | |
| Shift Left Logical | SLL | R | 010 | rs | rt | rd | sa | 010 |
| Shift Right Logical | SRL | R | 010 | rs | rt | rd | sa | 210 |
| Shift Left Logical Variable | SLLV | R | 010 | rs | rt | rd | 010 | 410 |
| Shift Right Logical Variable | SRLV | R | 010 | rs | rt | rd | 010 | 610 |

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| **Instruction name** | **Mnemonic** | **Format** | **Encoding** | | | | | |
| Move from HI | MFHI | R | 010 | 010 | 010 | rd | 010 | 1610 |
| Move to HI | MTHI | R | 010 | rs | 010 | 010 | 010 | 1710 |
| Move from LO | MFLO | R | 010 | 010 | 010 | rd | 010 | 1810 |
| Move to LO | MTLO | R | 010 | rs | 010 | 010 | 010 | 1910 |
| Multiply | MULT | R | 010 | rs | rt | 010 | 010 | 2410 |
| Multiply Unsigned | MULTU | R | 010 | rs | rt | 010 | 010 | 2510 |
| Divide | DIV | R | 010 | rs | rt | 010 | 010 | 2610 |
| Divide Unsigned | DIVU | R | 010 | rs | rt | 010 | 010 | 2710 |

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| **Instruction name** | **Mnemonic** | **Format** | **Encoding** | | | | | |
| Jump Register | JR | R | 010 | rs | 010 | 010 | 010 | 810 |
| Jump | J | J | 210 | instr\_index | | | | |
| Jump and Link | JAL | J | 310 | instr\_index | | | | |
| Branch on Equal | BEQ | I | 410 | rs | rt | offset | | |
| Branch on Not Equal | BNE | I | 510 | rs | rt | offset | | |